Optimization of 1700V 4H-SiC JBS Diode Parameters

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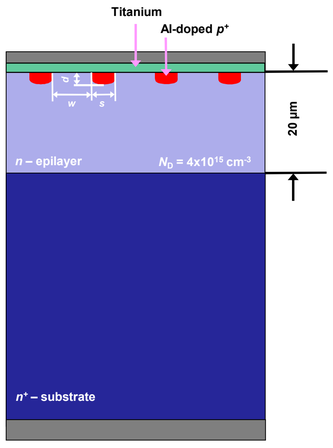
Aim

The aim of this work is a detailed design optimization of **the active layer of the 1700V class 4H-SiC JBS/MPS diode cell-architecture**. A systematic approach has been applied by taking into consideration all the parameters of strategic importance for the design such as **junction depth** (***d***), **width** (***w***) **of the *p*⁺ stripes**, and **spacing** (***s***) **between them**.

Experimental

The optimization is based on numerical simulations utilizing the drift-diffusion approximation of the finite-element device simulator ATLAS from Silvaco, Inc. Primarily, by utilization of the punch-through design for PiN and Schottky barrier diodes (SBD), the breakdown voltage (V_{BR}) limits for the junction barrier Schottky (JBS) diode have been defined. The thickness (t) and donor doping level (N_D) of the epitaxial-layer has been fixed to 20μm and 4×10^{15} cm^{-3} respectively to achieve a rectifier suitable for 1700V DC-link voltage. The optimized JBS structure consisted from alternating n-type (Schottky interface) and *p*⁺-type (p/n junction) areas covered by a Ti contact layer on top of the device. The p⁺-areas were formed by a multiple energy cascade Al implantation. The JBS architecture was placed on top of the n^- epitaxial layer grown on heavily doped 4H-SiC n^+ substrate. The calibration of our simulation models for different temperatures was performed using the experimentally measured forward and reverse static *I*-*V* characteristics. Our simulation results showed an excellent match to the experimental data, thus verifying that our models can be used for temperature dependent simulations of JBS/MPS rectifier architectures.



Optimization of Forward and Blocking Characteristics

Using a methodical approach for optimization, the key electronic characteristics such as forward conduction and reverse blocking and surge current behavior have been analyzed. First and foremost, the breakdown voltage (V_{BR}) and reverse current density (J_R) limits for the different JBS cell architectures have been defined using the punch-through design of PiN and SB diodes. The V_{BR} was defined as the voltage when J_R equals 1mA/cm². Results show that with increasing portion of the SBD area (w=1μm; s=1μm to 8μm) in the active region of the JBS diode decreases V_{BR} by about 1kV. At the same time, $J_R@V_R$=2kV increases about two orders of magnitude. At $s/w \geq 8$, the leakage of the JBS architecture approaches J_R of a pure SBD. On the other hand, the increasing shielding against the electric field (decreasing the s/w ratio) reduces the unipolar current handling capability of the JBS diode. In our case, the forward voltage drop $V_F@J_F$=200A/cm² increased from 1.90V (s/w=8) to 2.33V (s/w=1). The effect of the *p*⁺ depth (d) on both the OFF- and ON-state characteristics is not so pronounced, provided that the *p*⁺ regions don't get fully depleted up to avalanche breakdown. The increase of d only slightly decreases V_{BR} (the E_{max} increases due to the higher curvature of the *p*⁺ region) and increases V_F (due to lower conductivity of the Schottky-interface region). Similarly, the increase of the width (w) of the *p*⁺ regions reduces the unipolar conduction performance.

Optimization Results

Optimization results are shown as the dependencies of the optimization factor (V_{BR}/V_{FWD}) on the key parameter s/w (spacing/ *p*⁺-stripe width) for different values of w and d. The effect of temperature is also shown together with the optimization factor extracted from measurements on the commercial rectifier (magenta box, visualized by arrow). In principle, all evaluated data show a common trend which exhibits a maximum for s=2μm. For higher ratios of s/w, the V_{BR}/V_{FWD} decreases due to the decrease of the V_{BR}. A sharp decay in the V_{BR}/V_{FWD} at the low s/w side of the graph occurs when s decreases below 2μm. This shows that the proper spacing between *p*⁺ regions is the most crucial parameter. This is because, for narrow Schottky regions, the depletion width of the *p*⁺*n* junction becomes comparable to $s/2$ and consequently the path for current flow becomes very narrow. As a result, the JBS diode almost behaves like a PiN diode. The recommended value for s depends on the doping of the epitaxial layer N_D and for 1700V JBS design it should be between 2 to 4μm. The decrease of the implantation depth d slightly improves the V_{BR}/V_{FWD}, however it decreases the surge current capability. The temperature mainly affects the mobility of the electrons, therefore shifting the curve down.

Current Surge Capability

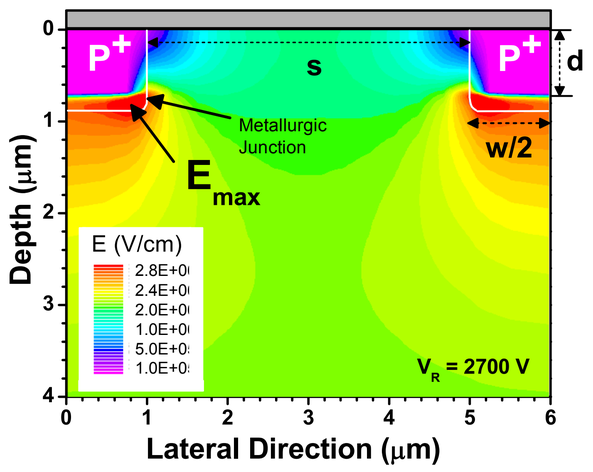
It is well known, that the JBS-architecture offers enhanced surge-current capability, when the minority-carrier injection of holes into the drift-layer by the *p*⁺ regions sets in at high current levels. in the ON-state. The impact of the design parameters (s, w, d) on the transition from unipolar to bipolar conduction is shown on right. Decreasing the doping level of the *p*⁺ regions slightly shifts the ignition of bipolar action towards higher ON-state voltages (not shown), whereas the depth of the *p*⁺ regions has a significant impact on the voltage igniting the bipolar action. The increase in temperature helps to inject holes at lower ON-state voltage and slightly decreases the peak forward voltage V_{Fmax}. The shift in the V_{Fmax} with temperature slightly decreases with decreasing d. The decrease of the s/w ratio is favorable for the surge current capability of the rectifier, since it decreases the voltage at which the hole-injection of *p*⁺ regions sets it. On the other hand, significant decrease of the s/w, deteriorates the ON-state characteristics in the unipolar regime. Therefore, the optimization of the depth of the *p*⁺ region and its shaping (decreasing of its curvature) can be a methodological approach to study the enhancement of the surge-current capability of the JBS power-rectifier. Finally, the effect of different profiles of *p*⁺ doping was investigated: box-like/multiple energy implantation (a), single energy implantation (b), different off-axis implantations (c-e). Results show that the shape of the profile has only a slight influence on the optimization factor, however, the metallurgical depth of the *p*⁺*n* junction significantly affects the voltage igniting the bipolar action.

Summary

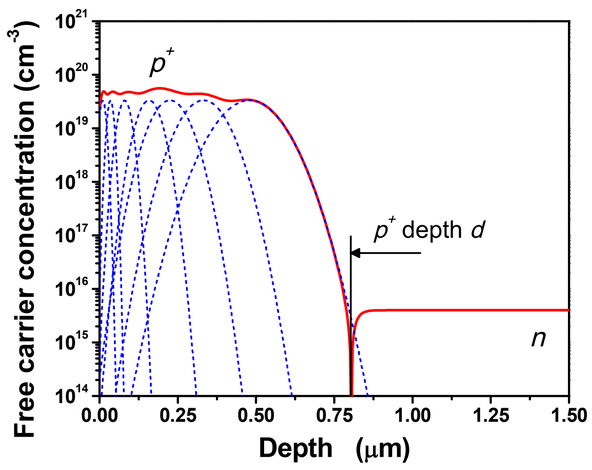
Systematic optimization of the active layer of the 1700V class 4H-SiC JBS/MPS diode cell-architecture by using calibrated TCAD models was presented. It is found that the spacing s between the *p*⁺ regions is the most decisive parameter which has to be properly chosen according to the required voltage class. For the 1.7kV voltage class, we found that s should be between 2 to 4 μm and the s/w ratio should be kept low. The *p*⁺ region depth d has significant impact on the ignition of bipolar action and with decreasing d, the surge current moderation capability suffers significantly. Due to the decrease of the built-in voltage, the increase in temperature by 100°C shifts the bipolar action towards lower ON-state voltages of about 0.5 V, which can be further reduced with decreasing of the *p*⁺*n* junction depth d.

Simulated Structure of the JBS Diode

Electric Field Distribution

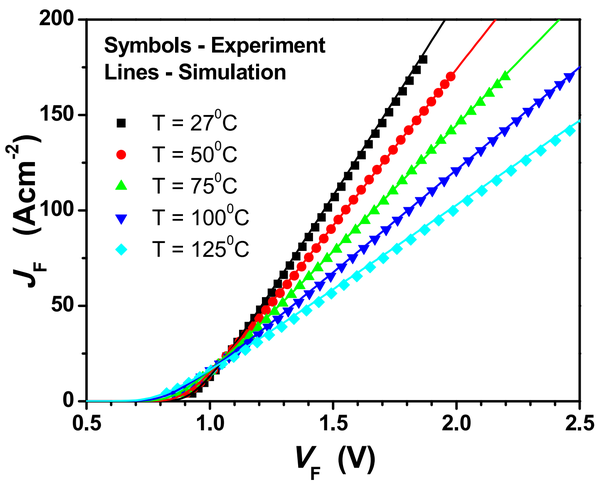


p⁺ Region Doping Depth Profile

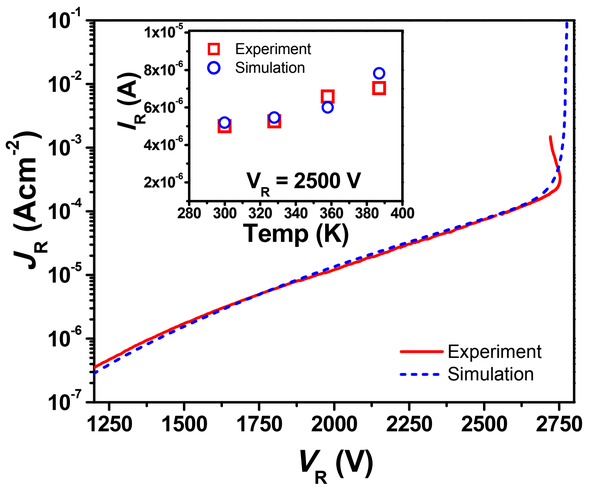


Calibration of the Simulation Model

Forward Characteristics

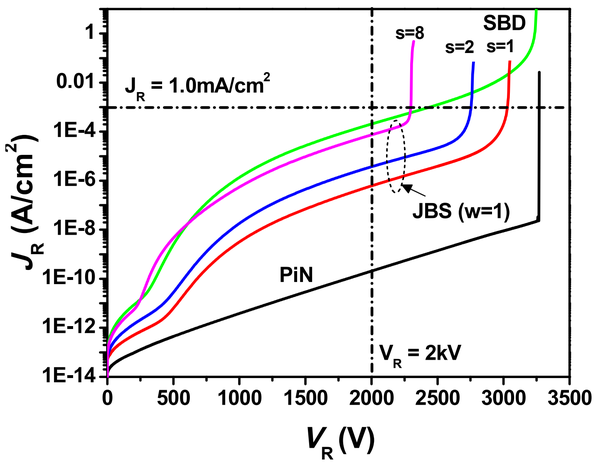


Blocking Characteristics

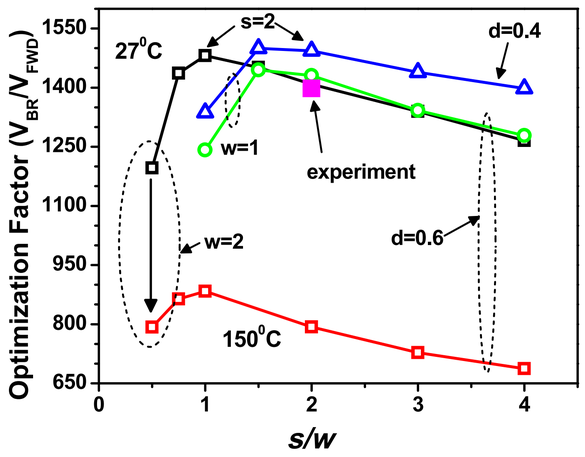


Impact of Design Parameters: *s*, *w* and *d*

OFF-State Characteristics - Effect of *s*/*w* Ratio

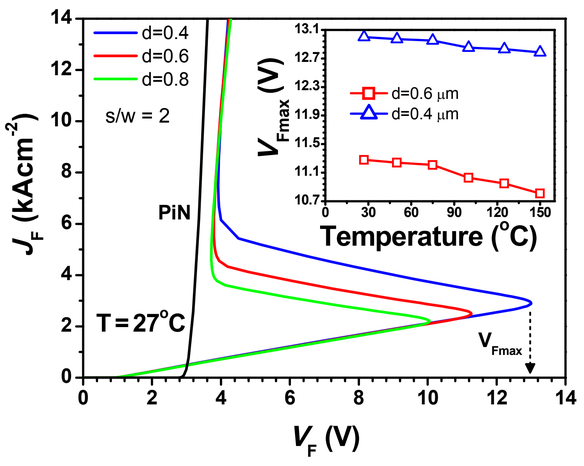


Optimization Factor - Effect of *s*, *w* and *d*

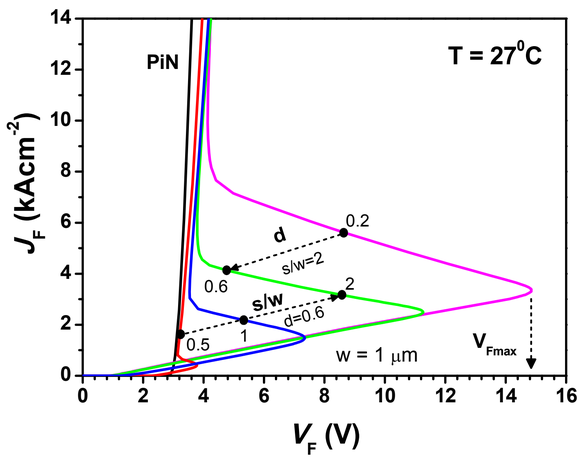


Surge-Current Capability

Impact of the *p*⁺ Region Depth *d*

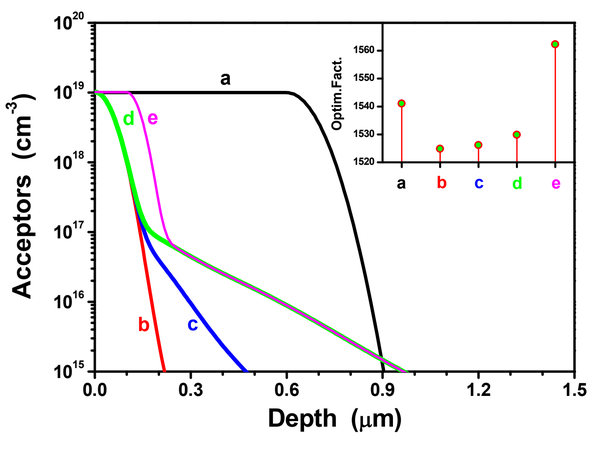


Impact of the Depth *d* and the *s*/*w* Ratio

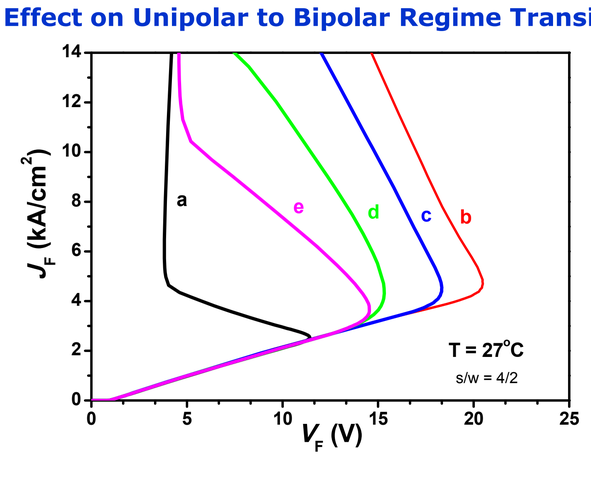


Effect of the *p*⁺ Region Profile Shape

Investigated Profiles of the *p*⁺ Region



Effect on Unipolar to Bipolar Regime Transition



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